Technical Note

CMOS LDO Regulators for Portable Devices

1ch 150mA CMOS LDO Regulators

BH□□SA3WGUT Series

No.11020EAT10

●Description

The BH□□SA3WGUT Series are 150 mA output CMOS regulators that deliver a highly stable output voltage with the precision of ± 1%. With the use of ROHM's original technology, the load regulation of only 2 mV, 100 mV I/O drop voltage, and the load transient of 50mV (at 1mA⇔100mA) have been achieved. The VCSP60N1 package is extremely compact as just 0.96 mm × 0.96 mm, and the IC's enhanced protection circuits contribute to improved application safety.

●Features

1) High accuracy output voltage: ± 1%
2) I/O drop voltage: 100 mV (at 100 mA)
3) Load Transient ⊿Vout : 50mV (at 1mA⇔100mA)
4) Stable with ceramic capacitors (1μF)
5) Low bias current: 40 μA
6) High ripple rejection ratio: 63 dB (Typ., 1 kHz)
7) Output voltage on/off control
8) Built-in overcurrent (short) and thermal shutdown circuits
9) Uses the VCSP60N1 WL-CSP package.

●Applications

Battery-driven portable devices, etc.

●Product Line

■150 mA BH□□SA3WGUT Series

Product name	1.8	2.8	3.0	Package
BH□□SA3WGUT	○	○	○	VCSP60N1

Model name: BH□□SA3W□
a b

Symbol	Description	
	Output voltage specification	
a	□□	Output voltage (V)
	18	1.8 V (Typ.)
	28	2.8 V (Typ.)
	30	3.0 V (Typ.)
b	Package GUT: VCSP60N1	

●Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Applied supply voltage	VMAX	-0.3 to +6.5	V
Power dissipation	Pd	530*1	mW
Maximum junction temperature	TjMAX	125	℃
Operating temperature range	Topr	-40 to +85	℃
Storage temperature range	Tstg	-55 to +125	℃

*1: Derated at 5.3 mW/℃ for temperature above Ta = 25℃, when mounted on a glass epoxy PCB (7 mm × 7 mm × 0.8 mm).

●Recommended Operating Ranges (not to exceed Pd)

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{IN}	2.2 to 5.5	V
Output current	IOUT	0 to 150	mA

●Recommended Operating Conditions

Parameter	Symbol	Ratings			Unit	Conditions
		Min.	Typ.	Max.		
Input capacitor	C_{IN}	0.5*2	1.0	—	μF	The use of ceramic capacitors is recommended.
Output capacitor	C_O	0.7*2	1.0	—	μF	The use of ceramic capacitors is recommended.

*2: The minimum value of capacitance must be met this specifications over full operating conditions.
(ex. Temperature, DC bias, aging conditions)

●**Electrical Characteristics** (Unless otherwise specified, Ta = 25℃, VIN = VOUT + 1.0 V*6, STBY = 1.5 V, CIN = 1 μF, CO = 1 μF)

Parameter		Symbol	Limits			Unit	Conditions
			Min.	Typ.	Max.		
Output voltage 1		VOUT1	VOUT × 0.99	VOUT	VOUT × 1.01	V	IOUT = 1 mA, Ta = 25℃, VOUT≧2.5V
			VOUT - 25 mV		VOUT + 25 mV		IOUT = 1mA, Ta = 25℃, VOUT＜2.5V
Output voltage 2		VOUT2	VOUT × 0.97	VOUT	VOUT × 1.03	V	IOUT = 0 to 150 mA VIN = VOUT+0.5V to 5.5V Ta = -40℃ to 85℃*3,4,5
Circuit current		IGND	—	40	72	μA	IOUT = 0 mA Ta = -40℃ to 85℃*4
Circuit current (STBY)		ICCST	—	—	1.0	μA	STBY = 0 V
Ripple rejection ratio		RR	50	63	—	dB	VRR = -20 dBv, fRR = 1 kHz, IOUT = 10 mA
Input output voltage difference		VSAT	—	100	150	mV	VIN = 0.98 × VOUT, IOUT = 100 mA (except BH18SA3WGUT)
Line regulation		VDLI	—	2	20	mV	IOUT = 10 mA VIN = VOUT + 0.5 V to 5.5 V*5
Load regulation1		VDLO1	—	2	30	mV	IOUT = 1 mA to 100 mA
Load regulation1		VDLO1	—	4	45	mV	IOUT = 1 mA to 150 mA
Maximum Output Current		IOMAX	150	—	—	mA	VIN = VOUT + 0.5 V*6
Limit current		ILMAX	—	400	—	mA	VO = VOUT × 0.98
Short current		ISHORT	—	50	200	mA	VO = 0 V
STBY pin current		ISTBY	0.5	1.3	3.6	μA	Ta = -40℃ to 85℃*4 IOUT = 150 mA
STBY control voltage	ON	VSTBH	1.2	—	VIN	V	
	OFF	VSTBL	-0.2	—	0.2	V	

*This product is not designed for protection against radio active rays.
*3: Operating condition are limited by Pd.
*4: Typical values apply for Ta=25℃.
*5: VIN=3.0V to 5.5V for BH18SA3WGUT.
*6: VIN=3.5V for BH18SA3WGUT.

●Reference data BH18SA3WGUT (Ta=25℃ unless otherwise specified.)

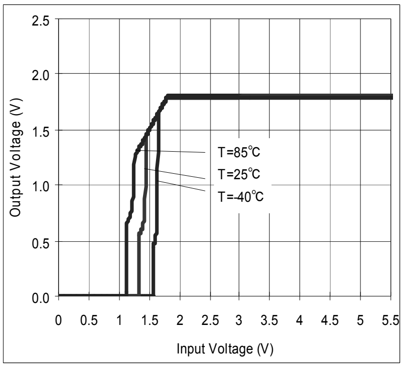


Fig.1 Output Voltage

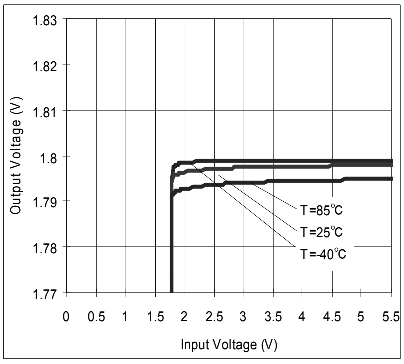


Fig.2 Line Regulation

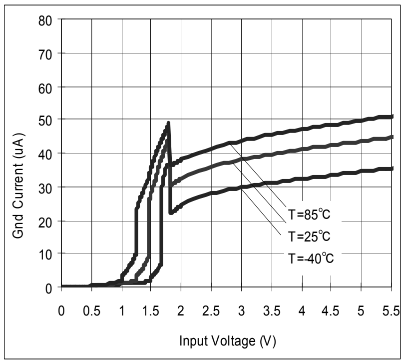


Fig.3 Circuit Current

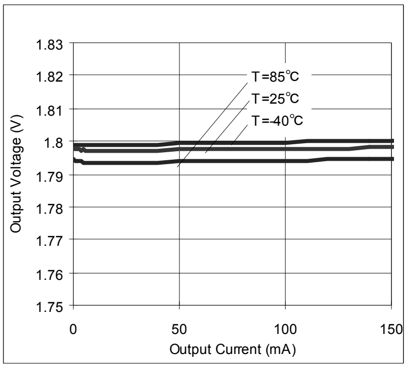


Fig.4 Load Regulation

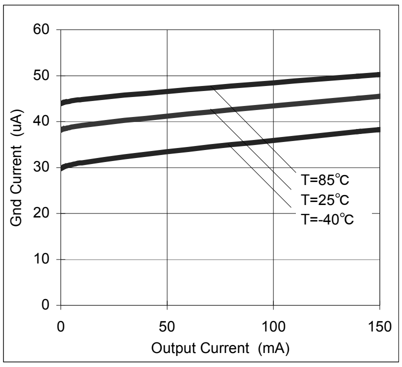


Fig.5 IOUT - IGND

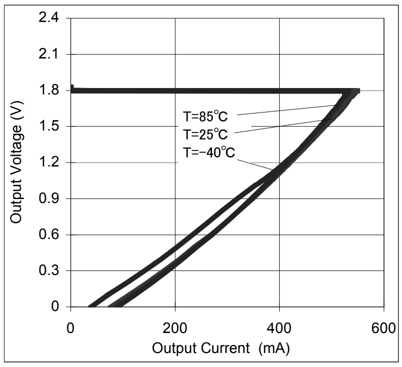


Fig.6 OCP Threshold

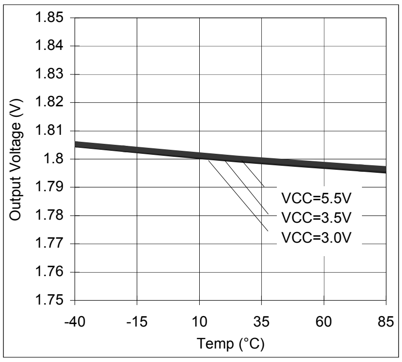


Fig.7 VOUT - Temp

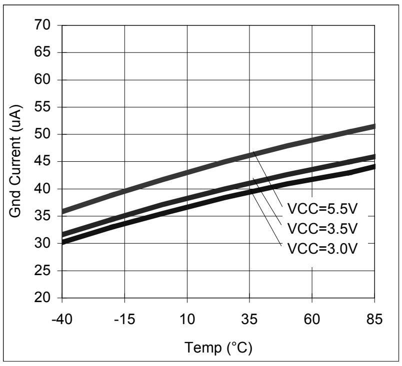


Fig.8 IGND - Temp

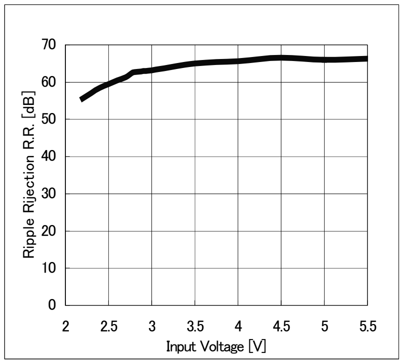


Fig.9 R.R. - VIN

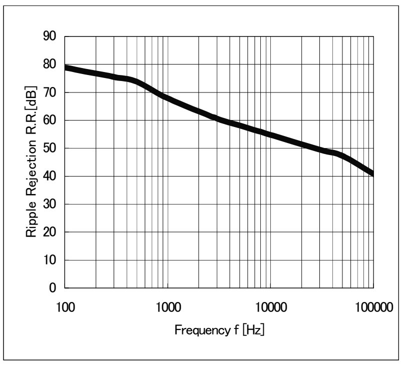


Fig.10 R.R. - Freq.

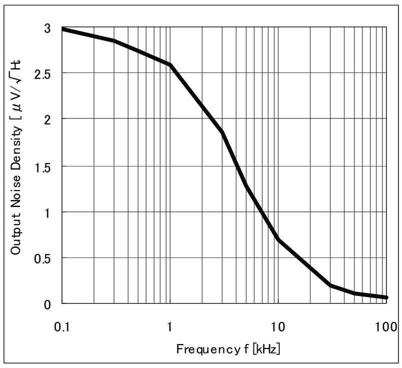


Fig.11 Noise - Freq.

●Reference data BH18SA3WGUT (Ta=25℃ unless otherwise specified.)

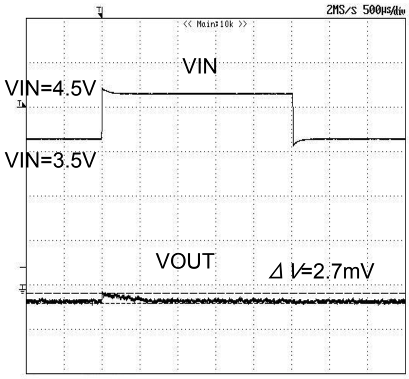


Fig.12 Transient_response (Ta=-40℃)

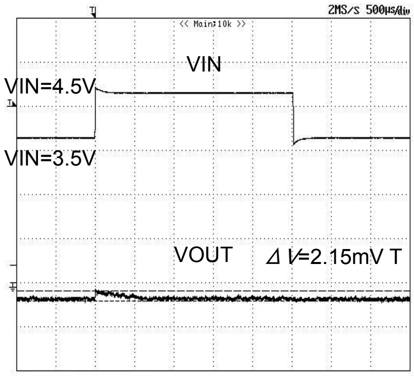


Fig.13 Transient_response (Ta=25℃)

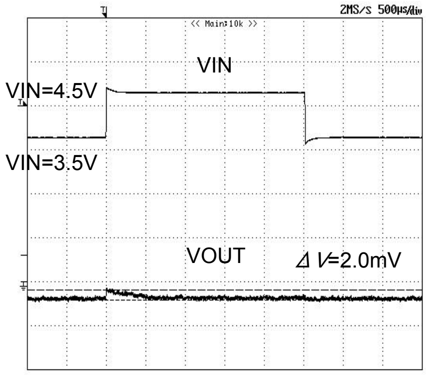


Fig.14 Transient_response (Ta=85℃)

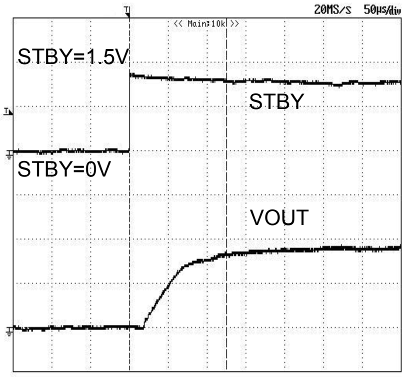


Fig.15 START_UP (Ta=-40℃)

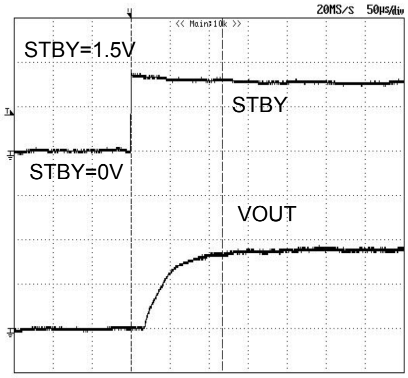


Fig.16 START_UP (Ta=25℃)

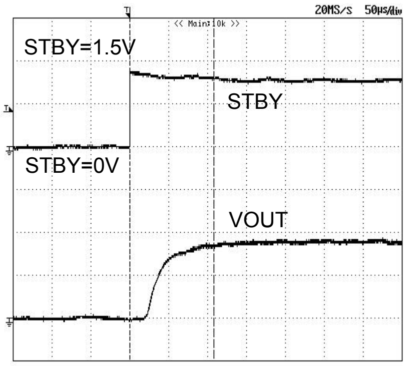


Fig.17 START_UP (Ta=85℃)

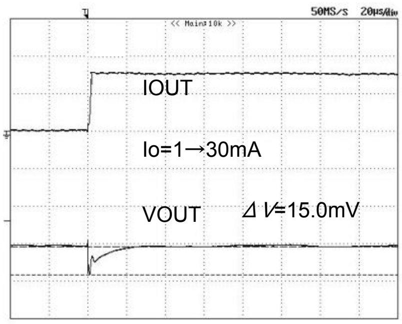


Fig.18 Load_response (Io=1→30mA) (Ta=-40℃)

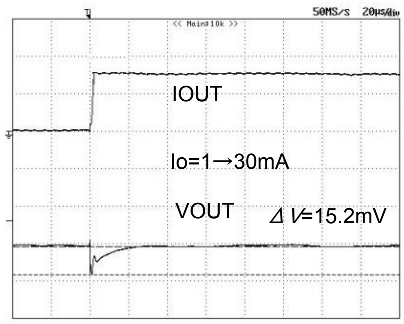


Fig.19 Load_response (Io=1→30mA) (Ta=25℃)

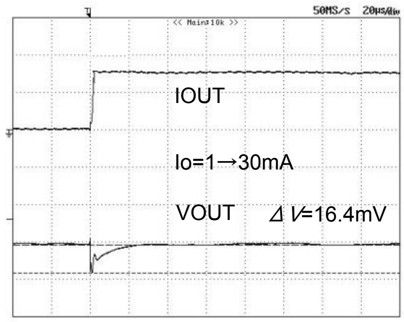


Fig.20 Load_response (Io=1→30mA) (Ta=85℃)

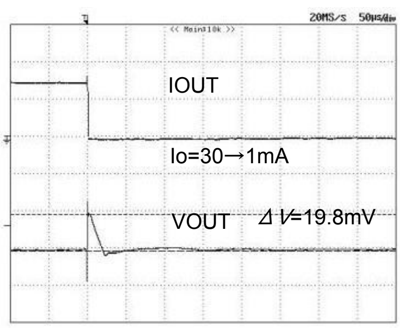


Fig.21 Load_response (Io=30→1mA) (Ta=-40℃)

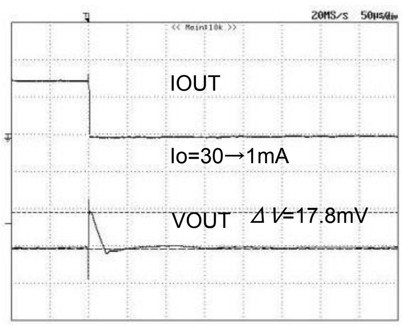


Fig.22 Load_response (Io=30→1mA) (Ta=25℃)

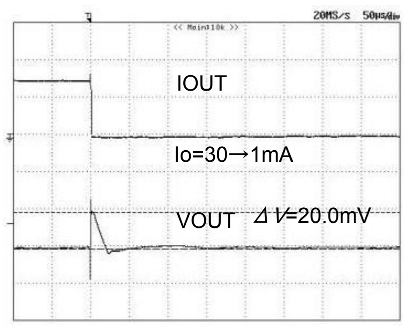


Fig.23 Load_response (Io=30→1mA) (Ta=85℃)

●Reference data　BH28SA3WGUT　(Ta=25℃ unless otherwise specified.)

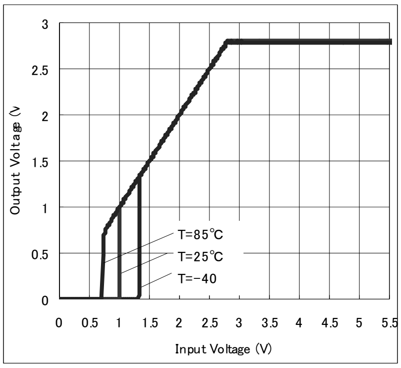


Fig.24　Output Voltage

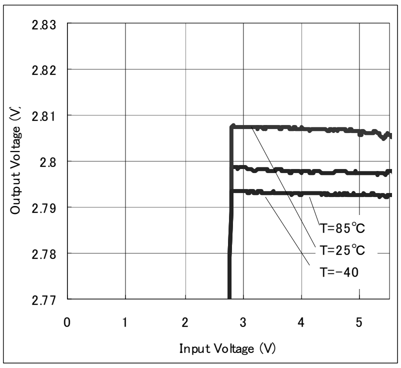


Fig.25　Line Regulation

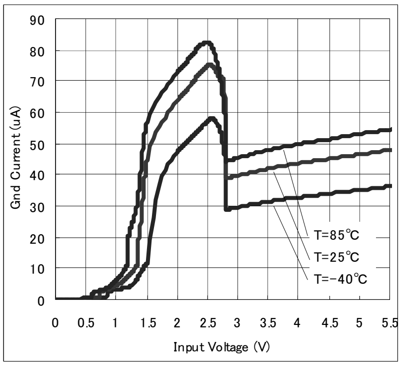


Fig.26　Circuit Current

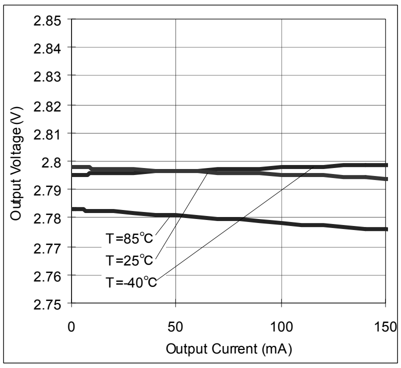


Fig.27　Load Regulation

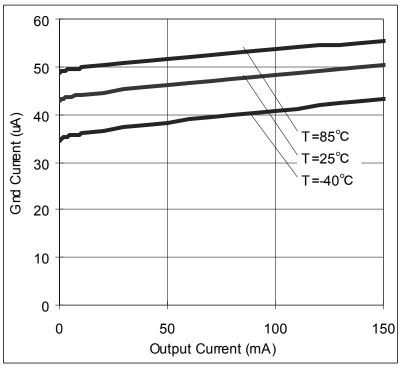


Fig.28　IOUT - IGND

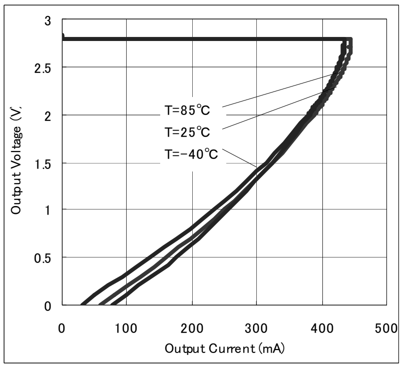


Fig.29　OCP Threshold

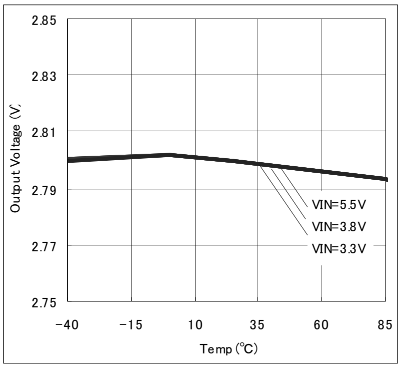


Fig.30　VOUT - Temp

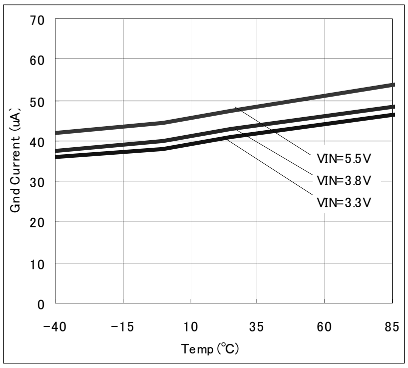


Fig.31　IGND - Temp

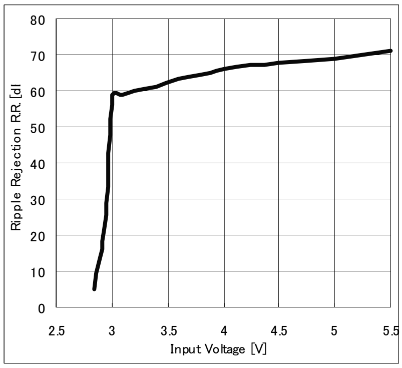


Fig.32　R.R. - VIN

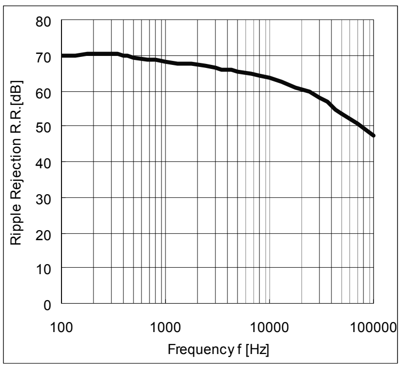


Fig.33　R.R. - Freq.

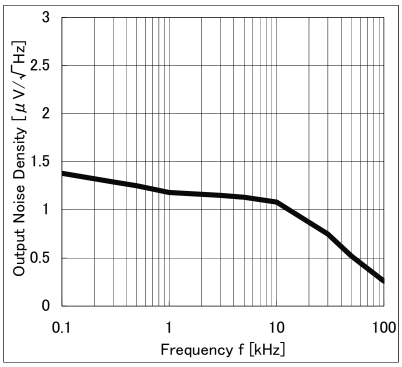


Fig.34　Noise - Freq.

●Reference data BH28SA3WGUT (Ta=25℃ unless otherwise specified.)

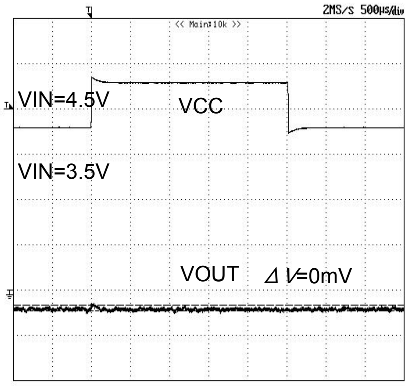


Fig.35 Transient_response
(Ta=-40℃)

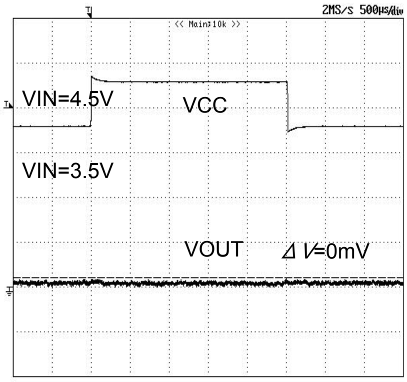


Fig.36 Transient_response
(Ta=25℃)

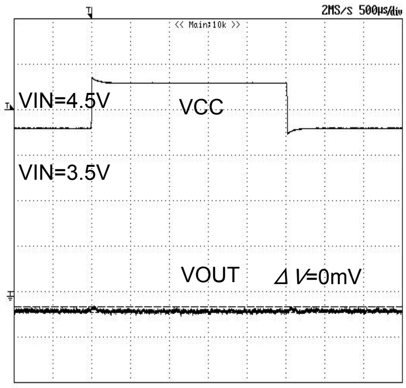


Fig.37 Transient_response
(Ta=85℃)

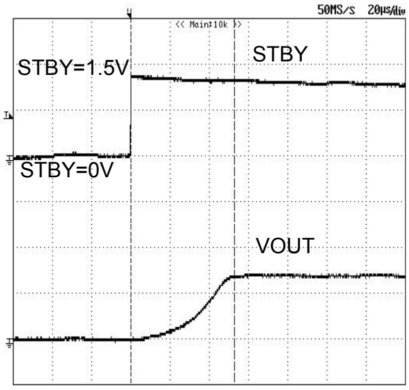


Fig.38 START_UP
(Ta=-40℃)

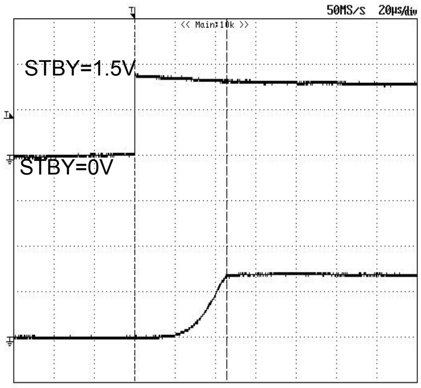


Fig.39 START_UP
(Ta=25℃)

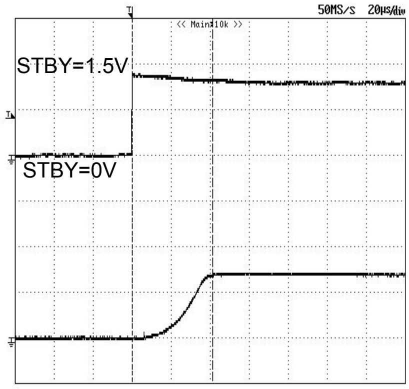


Fig.40 START_UP
(Ta=85℃)

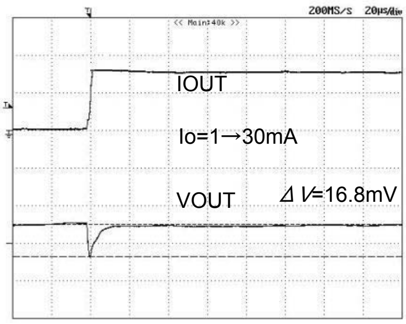


Fig.41 Load_response
(Io=1→30mA)
(Ta=-40℃)

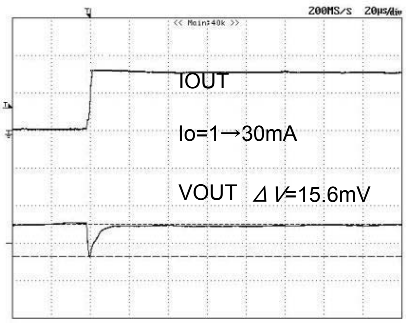


Fig.42 Load_response
(Io=1→30mA)
(Ta=25℃)

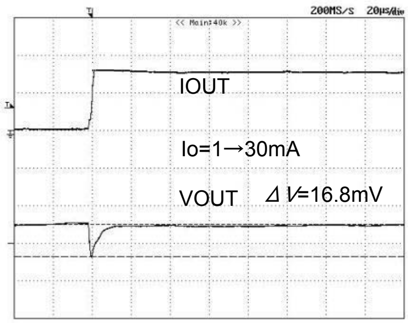


Fig.43 Load_response
(Io=1→30mA)
(Ta=85℃)

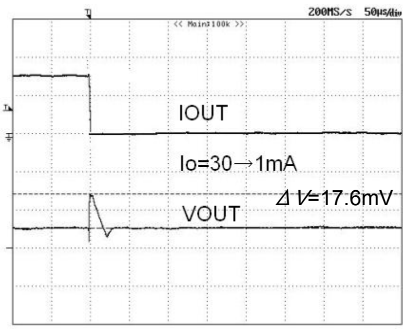


Fig.44 Load_response
(Io=30→1mA)
(Ta=-40℃)

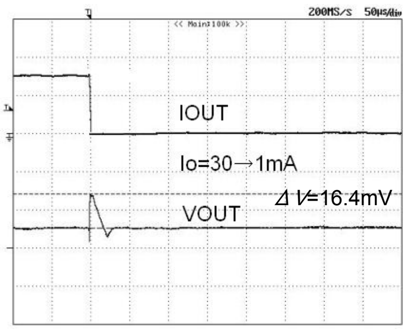


Fig.46 Load_response
(Io=30→1mA)
(Ta=25℃)

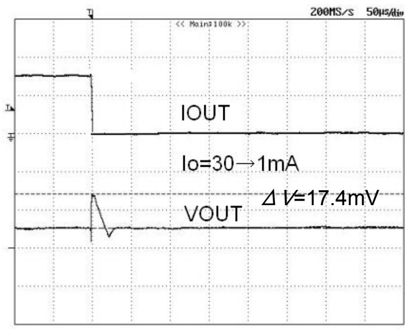


Fig.46 Load_response
(Io=30→1mA)
(Ta=85℃)

●Reference data BH30SA3WGUT (Ta=25℃ unless otherwise specified.)

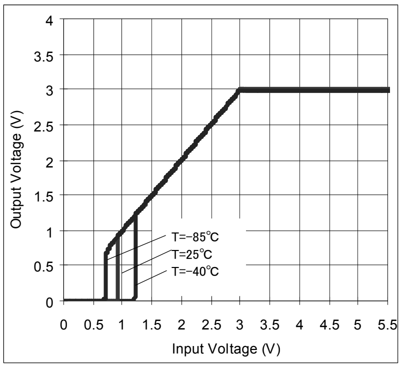


Fig.47 Output Voltage

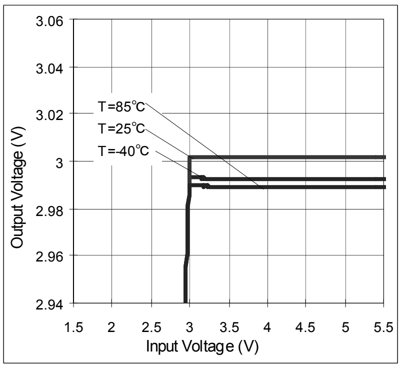


Fig.48 Line Regulation

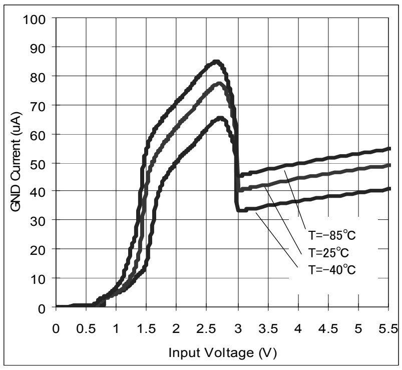


Fig.49 Circuit Current

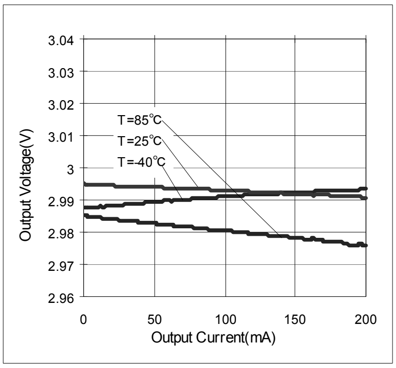


Fig.50 Load Regulation

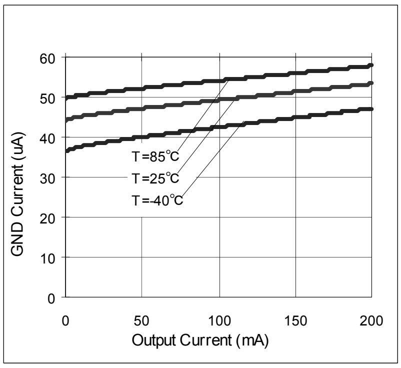


Fig.51 IOUT - IGND

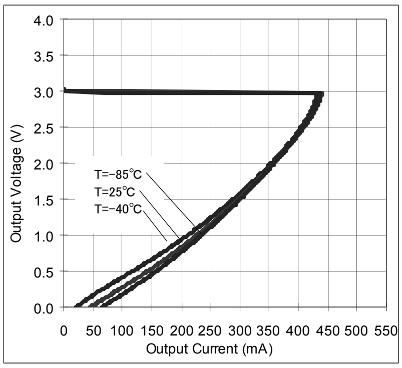


Fig.52 OCP Threshold

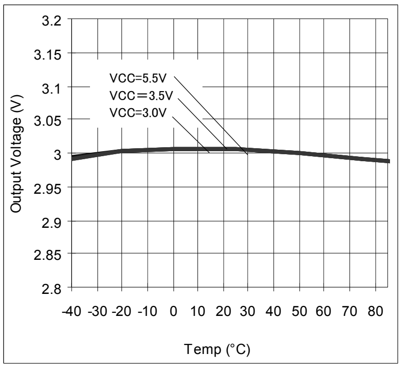


Fig.53 VOUT - Temp

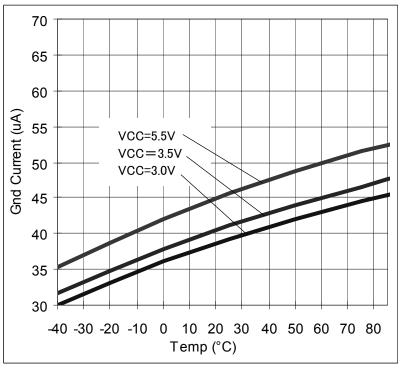


Fig.54 IGND - Temp

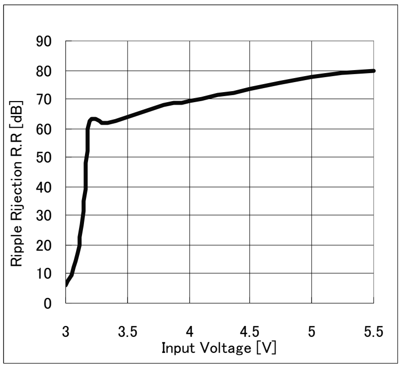


Fig.55 R.R. - VIN

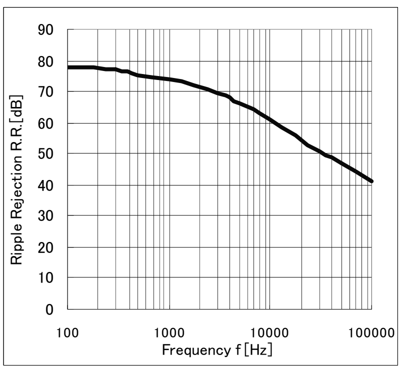


Fig.56 R.R. - Freq.

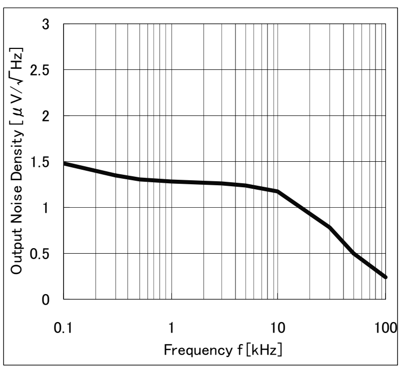


Fig.57 Noise - Freq.

●Reference data BH30SA3WGUT (Ta=25℃ unless otherwise specified.)

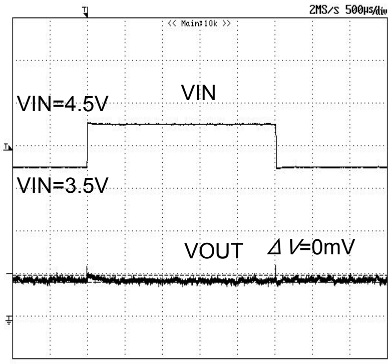


Fig.58 Transient_response
(Ta=-40℃)

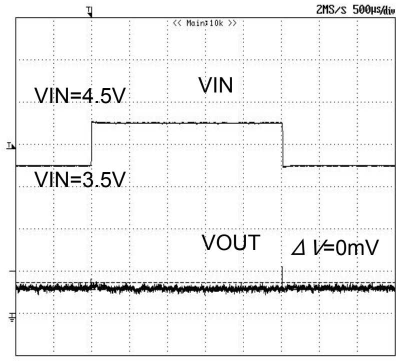


Fig.59 Transient_response
(Ta=25℃)

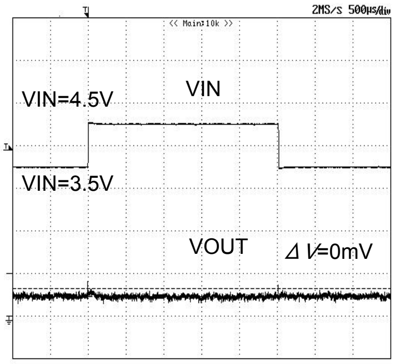


Fig.60 Transient_response
(Ta=85℃)

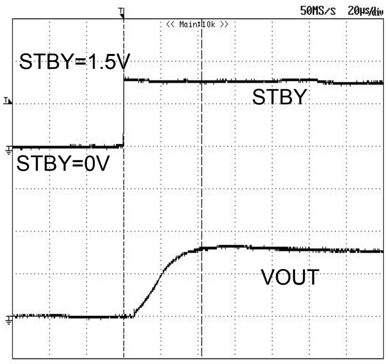


Fig.61 START_UP
(Ta=-40℃)

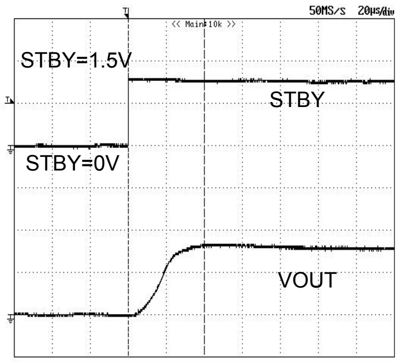


Fig.62 START_UP
(Ta=25℃)

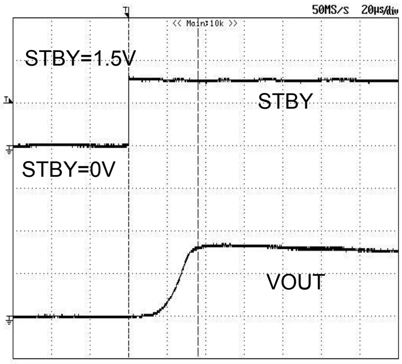


Fig.63 START_UP
(Ta=85℃)

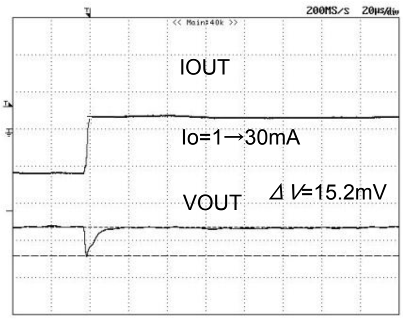


Fig.64 Load_response
(Ta=-40℃)
(Io=1→30mA)

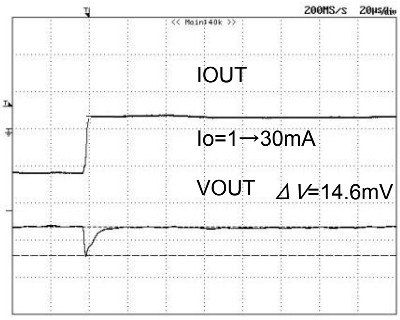


Fig.65 Load_response
(Ta=25℃)
(Io=1→30mA)

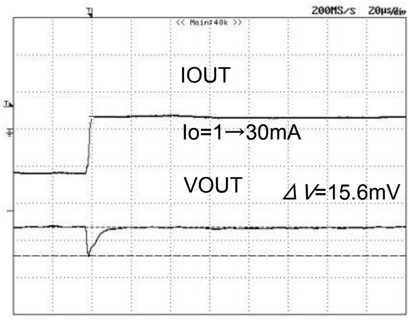


Fig.66 Load_response
(Ta=85℃)
(Io=1→30mA)

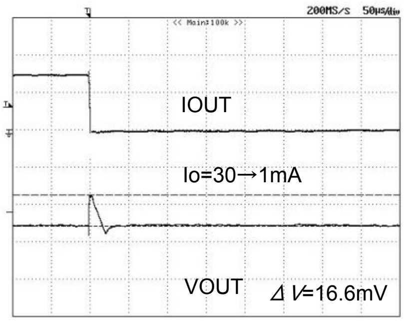


Fig.67 Load_response
(Ta=-40℃)
(Io=30→1mA)

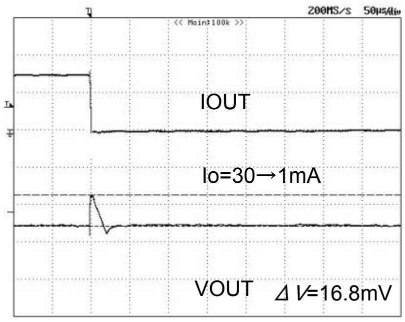


Fig.68 Load_response
(Ta=25℃)
(Io=30→1mA)

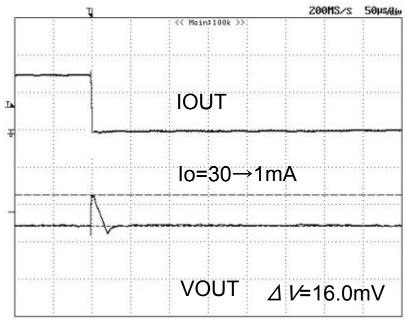
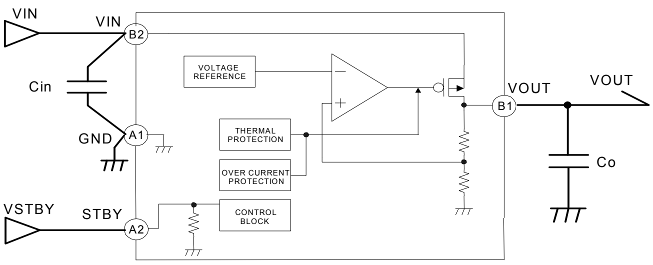


Fig.69 Load_response
(Ta=85℃)
(Io=30→1mA)

●Block Diagram, Recommended Circuit Diagram, and Pin Assignment Diagram

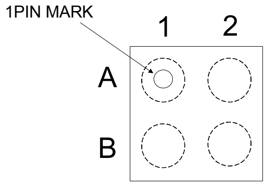
BH□□SA3WGUT



Cin: 1.0 μF
Co: 1.0 μF

Fig.70

Pin No.	Symbol	Function
B2	VIN	Power supply input
B1	VOUT	Voltage output
A1	GND	Ground
A2	STBY	Output voltage on/off control (High: ON, Low: OFF)



TOP VIEW (Mark side)

●Power Dissipation (Pd)

1. Power dissipation (Pd)
   Power dissipation calculations include estimates of power dissipation characteristics and internal IC power consumption and should be treated as rough guidelines. In the event that the IC is used in an environment where this power dissipation is exceeded, the attendant rise in the chip's temperature will trigger the thermal shutdown circuit, reducing the current capacity and otherwise degrading the IC's design performance. Allow for sufficient margins so that this power dissipation is not exceeded during IC operation.

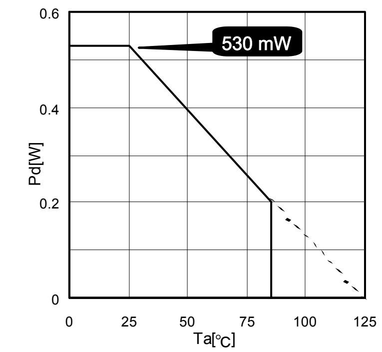
   Calculating the maximum internal IC power consumption (P_{MAX})

   PMAX = (VIN - VOUT) × IOUT (MAX.)

   VIN: Input voltage
   VOUT: Output voltage
   IOUT (MAX): Output current

2. Power dissipation/power dissipation reduction (Pd)

VCSP60N1



Board: 7 mm × 7 mm × 0.8 mm
Material: Glass epoxy PCB

Fig.71 VCSP60N1 Power Dissipation/Power Dissipation Reduction (Example)

*Circuit design should allow a sufficient margin for the temperature range so that P_{MAX} < Pd.

●Input Output Capacitors

It is recommended to insert bypass capacitors between input and GND pins, positioning them as close to the pins as possible. These capacitors will be used when the power supply impedance increases or when long wiring routes are used, so they should be checked once the IC has been mounted.
Ceramic capacitors generally have temperature and DC bias characteristics. When selecting ceramic capacitors, use X5R or X7R or better models that offer good temperature and DC bias characteristics and high torelant voltages.

Typical ceramic capacitor characteristics

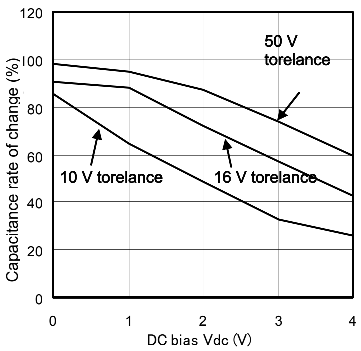


Fig.72 Capacitance vs Bias (Y5V)

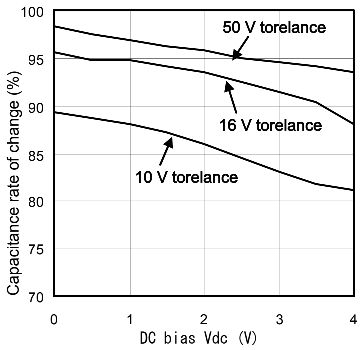


Fig.73 Capacitance vs Bias (X5R, X7R)

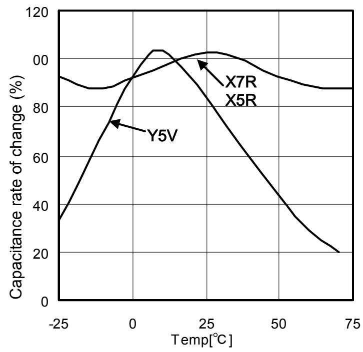


Fig.74 Capacitance vs Temperature (X5R, X7R, Y5V)

●Output Capacitors

Ceramic capacitors for stopping oscillation must be inserted between output and GND pins, positioned as close to the pins as possible. Larger output capacitance values provide greater stability as well as improved output load variation and other characteristics.

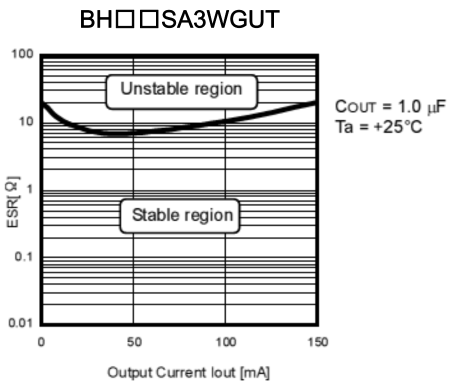


Fig.75 Stable Operating Region Characteristics (Example)

●Other Precautions

・Absolute maximum ratings
This product is subject to a strict quality management regime during its manufacture. However, damage may result if absolute maximum ratings such as applied voltage and operating temperature range are exceeded. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

・Setting of heat
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

・Pin short and mistake fitting
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC.

・Thermal shutdown circuit (TSD)
The IC incorporates a built-in thermal shutdown circuit. The thermal shutdown circuit is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of the thermal shutdown circuit is assumed.

・Overcurrent protection circuit
The IC incorporates a built-in overcurrent protection circuit that operates according to the output current capacity. This circuit serves to protect the IC from damage when the load is shorted. The protection circuits use fold-back type current limiting and are designed to limit current flow by not latching up in the event of a large and instantaneous current flow originating from a large capacitor or other component. These protection circuits are effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits.

・Actions in strong magnetic fields
Use caution when using the IC in the presence of a strong magnetic field as such environments may occasionally cause the chip to malfunction.

・Mutual impedance
Power supply and ground wiring should reflect consideration of the need to lower common impedance and minimize ripple as much as possible (by making wiring as short and thick as possible or rejecting ripple by incorporating inductance and capacitance).

・influence of strong light
Exposure of the IC to strong light sources such as infrared light from a halogen lamp may cause the IC to malfunction. When it is necessary to use the IC in such environments, implement measures to block exposure to light from the light source. During testing, exposure to neither fluorescent lighting nor white LEDs had a significant effect on the IC.

・GND potential
Ensure a minimum GND pin potential in all operating conditions.
In addition, ensure that no pins other than the GND pin carry a voltage less than or equal to the GND pin, including during actual transient phenomena.

● Back Current

In applications where the IC may be exposed to back current flow, it is recommended to create a route to dissipate this current by inserting a bypass diode between the V_{IN} and V_{OUT} pins.

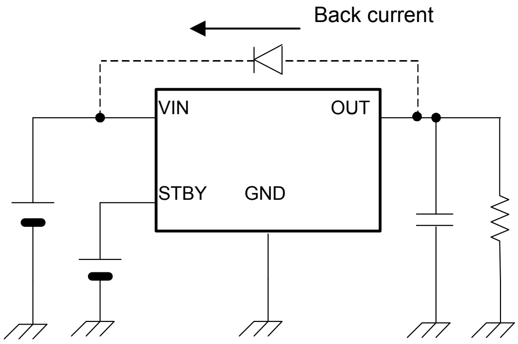


Fig.76 Example Bypass Diode Connection

● Testing on Application Boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

● Regarding Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.

For example, when a resistor and transistor are connected to pins as shown in Fig.77

- ○the P/N junction functions as a parasitic diode when GND > (Pin A) for the resistor or GND > (Pin B) for the transistor (NPN).
- ○Similarly, when GND > (Pin B) for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (P substrate) voltage to input pins.

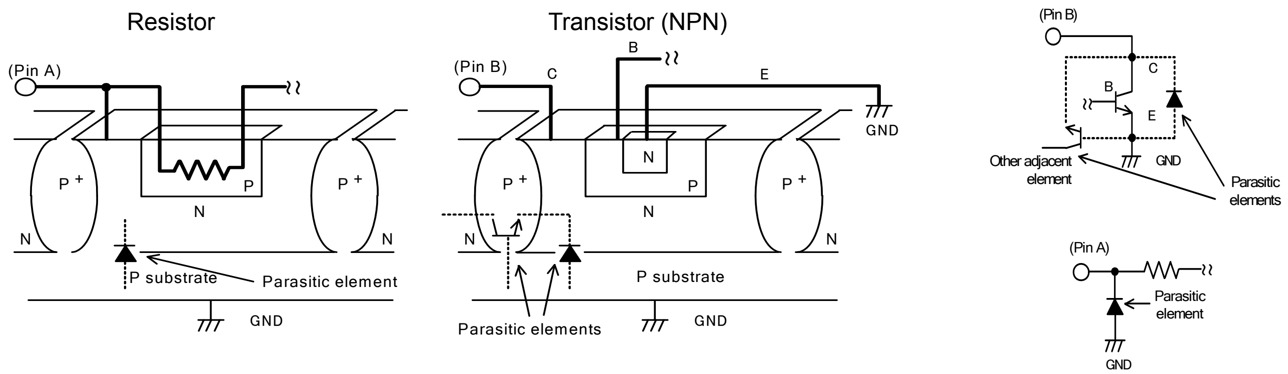
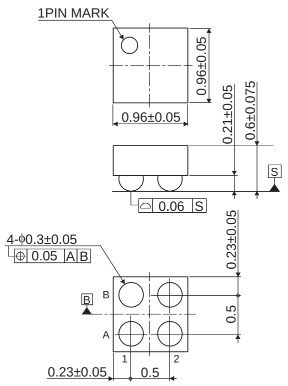


Fig.77

●Selecting a Model Name When Ordering

B H	1 8	S A 3	W	G U T	E 2
ROHM model name	Output voltage	Series Chip sizepackage	Shutdown switch	Packege GUT: VCSP60N1	Packaging and forming specification E2: Embossed tape and reel

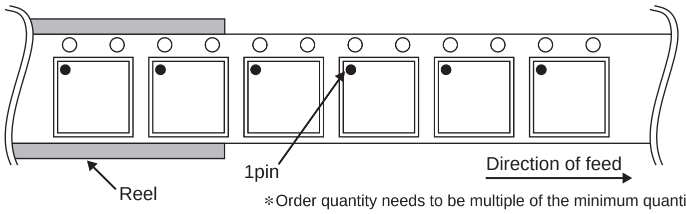
VCSP60L1(BHXXSA3WGUT)



(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape (heat sealing method)
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※Order quantity needs to be multiple of the minimum quantity.

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